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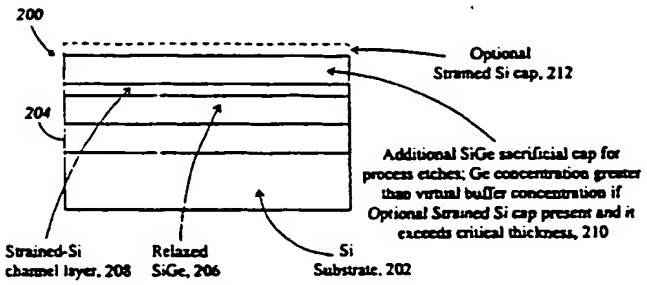
(54) Title: GATE TECHNOLOGY FOR STRAINED SURFACE CHANNEL AND STRAINED BURIED CHANNEL MOSFET DEVICES



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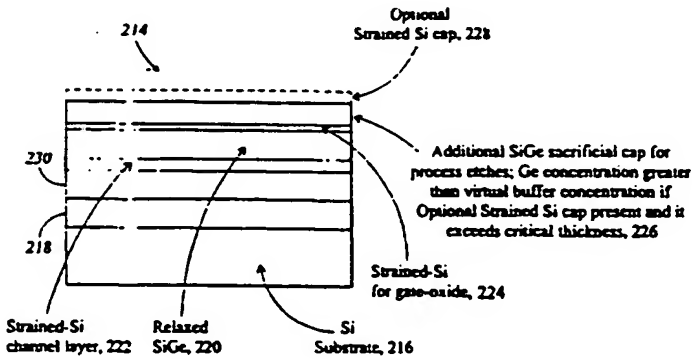

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(57) Abstract: A semiconductor structure including a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a sacrificial $Si_{1-y}Ge_y$ layer. The sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer. The dielectric layer includes a gate dielectric of a MOSFET. In alternative embodiements, the structure includes a $Si_{1-z}Ge_y$ spacer layer and a Si layer. In another embodiment of the invention there is provided a method of fabricating a semiconductor device including providing a semiconductor heterostructure, the heterostructure having a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on the relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer; removing the $Si_{1-y}Ge_y$ layer; and providing a dielectric layer.

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GATE TECHNOLOGY FOR STRAINED SURFACE CHANNEL AND STRAINED BURIED CHANNEL MOSFET DEVICES

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/223,595 filed August 7, 2000.

BACKGROUND OF THE INVENTION

The invention relates to gate technology for strained surface channel and strained buried channel MOSFET devices.

The advent of high quality relaxed SiGe layers on Si has resulted in the demonstration of field effect transistors (FETs) with carrier channels enhanced via strain. The strain can be incorporated in the channel due to the lattice mismatch between the channel and the relaxed SiGe created by a change in the Ge concentration between the channel layer and the relaxed SiGe layer. For example, a Ge concentration of 20% Ge in the relaxed buffer is high enough such that a thin strained Si layer can exhibit electron mobilities as high as1000-2900 cm^2/V-sec. Also, if the Ge concentration in the channel is greater than the concentration in the buffer, hole channel mobilities can be enhanced. For example, a relaxed buffer concentration of 60-70% Ge can compressively strain a Ge channel layer, creating potentially extremely high hole mobilities.

Although the exact physics of carrier scattering are not known inside short-channel FETs, one thing is clear: these enhanced mobilities translate into increased device performance, even at very short gate lengths. In addition to higher speed and a different power-delay product, the use of strained channels allows for the incorporation of new FET structures into Si-based circuits. Thus, it is anticipated that the high performance, new flexibility in device design, and economics of using a Si-based platform will lead to a plethora of new circuits and products.

With regards to these new circuits and products, the devices based on metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) gate technology are the most intriguing, since these devices can follow very closely the processes already used in Si VLSI manufacturing. Two main types of devices are of particular interest: the surface channel device and the buried channel device, examples of which are shown in

FIGs. 1A and 1B.

FIG. 1A is a cross section of a block diagram of a strained Si surface channel device 100, in which a thin strained Si layer 102 is grown atop a relaxed SiGe virtual substrate. The SiGe virtual substrate can be relaxed SiGe 104 on a SiGe graded buffer 105 (as shown in Figure 1a), relaxed SiGe directly on a Si substrate 106, or relaxed SiGe on an insulator such as SiO_2. The device also includes a SiO_2 layer 108 and gate material 110.

FIG. 1B is a cross section of a block diagram of a strained Si buried channel device 112, in which a SiGe layer 116 and a second strained Si layer 120 (used for gate oxidation) cap the strained Si channel layer 114. The structure also includes a graded SiGe buffer layer125 and a second relaxed SiGe layer 126. In both device configurations, a gate oxide 122 is grown or deposited and the gate material 124 is deposited to form the (MOS) structure. Although only devices with strained Si channels are shown in FIGs. 1A and 1B, the invention is applicable to any heterostructure device fabricated on a relaxed SiGe platform. For example, the heterostructure strained channel could be Ge or SiGe of a different Ge content from that of the underlying SiGe virtual substrate. However, the following description will focus on the applicability of the invention to the strained Si device variants illustrated in FIGs. 1A and 1B.

In order to form the MOS gate of the heterostructure device, the SiGe would ideally be oxidized directly in the buried channel device, and the strained Si would be oxidized directly in the surface channel device. Unfortunately, there are problems due to the nature of the Si/SiGe heterostructures in both cases that render the direct oxidation process unsatisfactory.

First consider the surface channel device. Since Si is being oxidized, the interface state density at the resulting SiO_2/Si interface is low, and an electrically high quality interface results. However, all oxidation and cleaning processes during the device and circuit fabrication consume the Si material. In conventional Si processing, there is generally little worry about Si consumption since so little material is consumed compared to any limiting vertical dimension early in the fabrication process. However, in the case of the strained surface channel FET described here, the top strained Si layer is typically less than 300Å thick, and thus too much Si consumption during cleaning and oxidation steps will eliminate the high mobility channel.

One obvious solution is to simply deposit extra Si at the surface, planning for the removal of the Si that occurs during processing. However, the channel strain, which gives the channel its higher carrier mobility, limits the Si layer thickness. At a great enough thickness, the Si layer will begin to relax, introducing misfit dislocations at the Si/SiGe interface. This process of dislocation introduction has two deleterious effects on device performance. First, the strain in the Si is partially or completely relieved, potentially decreasing the carrier mobility enhancements. Second, dislocations can scatter carriers, decreasing carrier mobility. Dislocations can also affect device yield, reliability, and performance.

The buried channel case appears to be a better situation at first, since the Si layer thickness is buried. However, in this case, direct oxidation of SiGe creates a very high interface state density at the oxide/SiGe interface, leading to poor device performance. A known solution in the field is to create a thin Si layer at the surface of the buried channel structure. In this structure, the surface layer is carefully oxidized to nearly consume the entire top Si layer. However, a thin layer of un-oxidized Si is left so that the interface to the oxide is the superior SiO_2/Si interface rather than the problematic oxide/SiGe interface. Although this sacrificial surface Si layer solves the interface electronic property issue, the structure now has the same limits as the structure described above, i.e., the sacrificial Si layer will be slowly etched away during Si processing, possibly leading to exposure of the SiGe and degradation of the electrical properties of the interface as described.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the invention there is provided a semiconductor structure including a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a sacrificial $Si_{1-y}Ge_y$ layer. In one aspect, the sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer. The dielectric layer includes a gate dielectric of a MISFET. In alternative embodiments the structure includes a $Si_{1-y}Ge_y$ spacer layer and a Si layer.

In accordance with another embodiment of the invention there is provided a method of fabricating a semiconductor device including providing a semiconductor heterostructure, the heterostructure having a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a

strained channel layer on the relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer; removing the $Si_{1-y}Ge_y$ layer; and providing a dielectric layer. The dielectric layer includes a gate dielectric of a MISFET. In alternative embodiments, the heterostructure includes a SiGe spacer layer and a Si layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A and 1B are cross sections of block diagrams of strained Si surface and buried channel devices, respectively;

FIGs. 2A and 2B are cross sections of block diagrams of starting heterostructures for surface channel and buried channel strained MOS, respectively, in accordance with the invention;

FIGs. 3A–3D are block diagrams showing the process sequence for a strained surface channel MOS device;

FIGs. 4A-4D are block diagrams showing the process sequence utilizing the gate structure for a buried channel device;

FIG. 5 is a graph of oxidation rates, under a wet oxidation ambient at 700°C, of SiGe alloys, with Ge contents of 0.28 and 0.36, compared to the oxidation rate of bulk silicon;

FIG. 6 is a graph showing the oxide thickness of both a $Si_{0.7}Ge_{0.3}$ alloy and a Si/$Si_{0.7}Ge_{0.3}$ heterostructure;

FIG. 7 is a cross-sectional transmission electron micrograph (XTEM) of the Si/$Si_{0.7}Ge_{0.3}$ heterostructure;

FIG. 8 is a XTEM image of the identical Si/$Si_{0.7}Ge_{0.3}$ heterostructure after wet oxidation followed by oxide removal via a wet etch;

FIG. 9 is a structure for a buried channel MOSFET using relaxed SiGe and strained Si in accordance with the invention; and

FIG. 10 is a graph showing a plot of the middle SiGe layer thickness (h2) and the resulting misfit dislocation spacing.

DETAILED DESCRIPTION OF THE INVENTION

To eliminate the issue of losing valuable surface Si, an innovative step that has

not been previously considered can be employed. In fact, any interest in this area is dominated by discussions of how to change the Si device and circuit process to conserve Si consumption. Although these are certainly possibilities, such constraints severely limit process flexibility, alter the process further from the conventional Si process, and most likely will increase the cost of the fabrication process.

A solution for the buried channel and surface channel structures is to actually deposit another SiGe layer after the desired device structure (which, in the buried channel heterostructure, includes the sacrificial Si layer for oxidation). The structures are shown in FIGs. 2A and 2B.

FIG. 2A is a cross section of a block diagram of a starting heterostructure 200 for surface channel strained MOS in accordance with the invention. The structure 200 includes a Si substrate 202, a SiGe graded buffer 204, a relaxed SiGe layer 206, and a strained-Si channel layer 208. FIG. 2B is a cross section of a block diagram of a starting heterostructure 214 for buried channel strained Si MOS. The structure 214 includes a Si substrate 216, a SiGe graded buffer 218, relaxed SiGe layers 220 and 230, a first strained-Si channel layer 222 and a second strained-Si layer 224 for the gate oxide.

These structures are identical to those depicted in FIGs. 1A and 1B before the gate stack formation, except for the addition of a SiGe capping layer 210, 226 and an optional Si capping layer 212, 228. Since the SiGe layer 210, 226 is closely lattice-matched to the relaxed SiGe layer below the device layers, there is essentially no limit on the thickness of the SiGe layer. This SiGe layer thickness can be tuned to the thickness of material removed before gate oxidation, so that the strained Si layer is exposed just before oxidation. Alternatively, the SiGe can be thicker than the removal thickness and then can be selectively removed. In fact, as described below, SiGe can be selectively removed with respect to Si using a variety of conventional Si-based processes. Therefore, cleaning and oxidation steps can be performed during the Si device and circuit fabrication process with little worry of consuming the precious strained Si and/or the sacrificial strained Si. One only needs to create a SiGe thick enough such that it is not totally consumed before the critical gate oxidation step.

An additional option can be to place yet another Si layer 212, 228 on top of the additional SiGe layer 210, 226. In some processing facilities, the idea of SiGe on the surface, instead of Si, is a factor for concern. In this case, another Si layer can be

deposited on top of the additional SiGe layer described above. By choosing the Ge concentration in the additional SiGe layer to be greater than that of the virtual buffer, a compressive layer can be created; thus, if this additional optional Si layer is greater than the critical thickness, there is no possibility of dislocations moving into the device layers. This phenomenon occurs since the Si layers are tensile, and therefore dislocations introduced into the top optional Si layer have a Burgers vector that will not allow them to glide favorably in the compressive layer below. The dislocations in the top optional Si layer (if the Si layer critical thickness is exceeded) will not penetrate into the layers beneath it, and therefore as much Si can be deposited as desired. In fact, this optional Si capping layer need not be strained at all in this case and can serve as a protective sacrificial layer even if it is fully relaxed.

FIGs. 3A–3D are block diagrams showing the process sequence for a strained surface channel MOS device utilizing the gate structure described above (the process is shown for a structure without an optional strained surface layer). FIG. 3A shows the initial Si/SiGe heterostructure 200 shown in FIG. 2A. FIG. 3B shows the structure after the completion of the initial steps of a Si VLSI process, which could include wet chemical cleans and oxidation steps. Thus, in FIG. 3B, the protective SiGe capping layer 210 has been reduced in thickness, as a portion of the layer has been consumed during processing. Next, the remainder of the protective SiGe capping layer 210 is selectively removed, leaving the underlying Si layer 208 intact and exposed. A sacrificial oxidation step and oxide strip can also be performed at this point to improve the quality of the exposed Si surface.

The resulting structure is shown in FIG. 3C. FIG. 3D shows the final device structure after gate oxidation to form a gate oxide 300, a structure in which the minimum possible amount of Si was consumed prior to the gate oxidation step. Alternatively, at this point an alternate gate dielectric could be deposited on the exposed Si surface. A pristine Si surface is just as important for a high quality interface with many deposited gate dielectrics as it is for a thermally grown SiO_2 gate dielectric.

FIGs. 4A-4D are block diagrams showing the process sequence utilizing the gate structure for a buried channel device (the process is shown for a structure without an optional strained surface layer) using the initial Si/SiGe heterostructure 214 shown in FIG. 2B. The process steps are identical to those of FIGs. 3A-3D, but in the final

heterostructure, the Si channel layer 222 is separated from the gate dielectric 400 by a SiGe spacer layer 220, thus forming a buried channel. Using selective processes to etch down to the buried Si channel or the top Si layer can use the starting heterostructure 214 in FIG. 4A to form a surface channel device. Such a process can result in enhancement mode and depletion mode devices that can in turn be used to create E/D logic circuits as well as a plethora of analog circuits.

In both sequences, an exemplary sequence of steps is: 1. Pre-gate-oxidation cleaning steps and oxidation; 2. Selective etch or oxidation to remove residual protective SiGe layer; 3. Sacrificial oxide formation on Si; 4. Sacrificial oxide strip; 5. Gate oxidation.

It will be appreciated that steps 3 and 4 can be optional, depending on whether there may be a small amount of Ge left on the surface after the selective removal of the SiGe protection layer. When the original heterostructure is grown, the SiGe/Si interface will not be infinitely abrupt, and therefore it is possible to have a small amount of Ge in the optimally pure Si layer. A sacrificial oxide step can be employed to remove an additional small amount of the Si layer to ensure that pure Si is oxidized in the gate oxidation step, ensuring high quality gate oxide.

The second step, the selective removal of the residual SiGe protective material, can be accomplished in a variety of ways. One convenient process is a wet oxidation step, preferably at 750°C or below. Under wet oxidation at these temperatures, SiGe is oxidized at rates that can be 100 times greater than rates oxidizing Si under the same conditions. Thus, in order to expose the Si for gate oxidation, one can simply do a wet oxidation of the SiGe layer and selectively stop at the Si layer. The oxidized SiGe can be stripped to expose the Si. It is important to note here that the low temperature is not only important for the selectivity in the oxidation process, but also the low temperature is important to minimize or prevent the snow-plowing of Ge in front of the oxidation front, a known problem in the direct oxidation of SiGe.

FIG. 5 is a graph of oxidation rates, under a wet oxidation ambient at 700°C, of SiGe alloys, with Ge contents of 0.28 and 0.36, compared to the oxidation rate of bulk silicon. It is evident from the graph that, under such conditions, the oxidation rate of SiGe increases as the Ge content of the film increases.

FIG. 6 is a similar graph, showing the oxide thickness of both a $Si_{0.7}Ge_{0.3}$ alloy and a Si/ $Si_{0.7}Ge_{0.3}$ heterostructure. Again, the oxidation conditions were 700 C in a

wet ambient; however, FIG. 6 depicts very short oxidation durations compared to FIG. 5. The Si/ $Si_{0.7}Ge_{0.3}$ heterostructure consists of a 50Å strained Si buried layer, followed by a 30Å $Si_{0.7}Ge_{0.3}$, a 20Å strained Si layer and finally a 50Å $Si_{0.7}Ge_{0.3}$ capping layer.

A cross-sectional transmission electron micrograph (XTEM) of the $Si/Si_{0.7}Ge_{0.3}$ heterostructure is shown in FIG. 7. It should be noted from FIG. 6 that the presence of strained Si layers in the heterostructure results in a dramatic retardation in the oxidation rate when compared to the oxidation rate of the uniform $Si_{0.7}Ge_{0.3}$. This retardation of the oxidation rate forms the basis of the selective removal of SiGe alloys over strained Si epitaxial layers.

FIG. 8 is a XTEM image of the identical $Si/Si_{0.7}Ge_{0.3}$ heterostructure after wet oxidation at 700°C for 2 minutes followed by oxide removal via a wet etch. It is apparent that the thin strained Si layer is unaffected by the selective oxidation and remains fully intact. Based on the data shown in FIG. 5, an oxidation duration of 2 minutes far exceeds that required to fully oxidize the 50Å $Si_{0.7}Ge_{0.3}$ capping layer of the heterostructure. The very thin dark band, which is apparent on the surface of the strained Si layer, is a snow-plowed high Ge content layer that occurs during oxidation. Such a layer may be removed using a simple chemical clean or a sacrificial oxidation step, either or both of which typically occur prior to the formation of the gate oxide.

Alternatively, the protective SiGe capping layer can be removed via selective dry or wet chemical etching techniques. For example, at high pressures (>200mT) and low powers, CF_4 dry etch chemistries will etch relaxed SiGe films with high selectivity to Si. Mixtures of hydrofluoric acid (HF), hydrogen peroxide (H_2O_2), and acetic acid (CH_3COOH) will also selectively etch relaxed SiGe layers over Si at selectivities of 300:1 or more. Other potential selective wet chemical mixtures include HF, water (H_2O), and either H_2O_2 or nitric acid (HNO_3).

Additionally, the stability of the entire structure can be improved by increasing the Ge concentration in the intermediate SiGe layer, and also the top SiGe layer if desired. Below, energetic calculations are used to reveal a guide to creating semiconductor layer structures that increase stability with respect to misfit dislocation introduction.

The critical thickness for a buried channel MOSFET using relaxed SiGe and strained Si has been determined using the energy-balance formulation. The structure

considered is the one shown in FIG. 9. The structure 900 includes a 30% SiGe virtual substrate 902 topped by a 80Å strained Si layer 904, a SiGe layer with Ge concentration x2 and thickness h2 906, and an additional 30Å of strained Si 908. Additional stability would result from the addition of an additional SiGe cap layer as described previously. To simplify, the example of FIG. 9 considers only the increased stability created by increasing the Ge concentration (x2) or thickness (h2) of the SiGe intermediate layer. Additionally, since the SiGe cap layer is removed during processing, the stability of the heterostructure with the SiGe cap removed is or primary importance.

In device processing, one must consider the critical thickness of the entire structure with respect to the relaxed virtual substrate. Individual layers that exceed the individual critical thicknesses are not explicitly ruled out, so one practicing the art would have to verify that none of the layers that are introduced into the desired structure exceed the individual layer critical thicknesses. In other words, in the following calculation it is assumed that each layer in the structure is below its critical thickness with respect to the relaxed buffer.

One key to the formulation is to realize that this calculation should be done with respect to the plastic deformation of the layer composite, δ. Then, the dislocation array energy is the same expression regardless of the layer structure. The elastic energy in the individual layers is changed because of δ. In tensile layers, the strain is lowered by δ. In compressive layers, the energy is raised by δ.

Thus, the energy for a dislocation array (per unit area) inserted at the base of the composite is:

$$E_\delta = 2\delta D(1-\nu\cos\alpha)[\ln(h_T/b)+1]$$

where h_T is the total thickness of the composite ($h_1+h_2+h_3$), α is the angle between the dislocation line and the Burgers vector b, ν is the Poisson ratio, and D is the average shear modulus for a dislocation lying at the interface between the virtual substrate and the composite structure.

The total elastic energy (per unit area) in all the layers is:

$$E_\varepsilon = \sum_{i=1}^{3} Y\varepsilon_i^2 h_i$$

where Y is the Young's modulus. Thus, the total energy of the system is:

$E_T = E_\delta + E_\varepsilon$.

The energy can now be minimized with respect to δ (if the energy is lowest with no dislocations, then δ will have a less than or equal to zero value). The value of plastic deformation then is (for the 3 layer example):

$$\delta = \frac{f_1 h_1}{h_T} - \frac{f_2 h_2}{h_T} + \frac{f_3 h_3}{h_T} - \frac{D(1-\upsilon\cos^2\alpha)\left[\ln\left(\frac{h_T}{b}\right)+1\right]}{Y h_T}$$

The examination of this solution reveals that a general formulation for any structure would be (for any structure of n layers):

$$\delta = \sum_i^n \frac{f_i h_i}{h_T} - \frac{D(1-\upsilon\cos^2\alpha)\left[\ln\left(\frac{h_T}{b}\right)+1\right]}{Y h_T}$$

where f has been assigned a negative value for compressive layers and positive value for tensile layers, and hT is the total thickness of the structure:

$$h_T = \sum_i^n h_i .$$

The amount of plastic deformation and resulting misfit dislocation spacing S was calculated for the structure depicted in FIG. 9 as follows:

Lower strained Si layer thickness h1=80Å

Upper strained Si layer thickness h3=30Å

Middle SiGe layer thickness h2 variable

Middle SiGe layer Ge concentration x2 variable

Virtual substrate Ge concentration: 30%

FIG. 10 is a graph showing a plot of the middle SiGe layer thickness (h2) and the resulting misfit dislocation spacing. The sharp upturn on the plots represents the critical thickness h2 of the middle SiGe layer when the entire composite structure destabilizes and introduces dislocations at the channel/virtual buffer interface. The different curves are for the different compositions in the second layer h2. Very small increases in Ge result in a large jump in stability of the device layers. This suggests that it is possible to stabilize the layer significantly but not have the band structure altered that much. Adding an extra 5-10% Ge into the h2 layer increases the stability

drastically. For example, FIG. 10 indicates that over 100Å of 30% Ge is required to provide the stability of a 20Å layer of 45% Ge content.

Increasing h2 even when the h2 layer is lattice-matched to the virtual buffer increases the stability of the multilayer structure. In the equations above, the effect can be seen to be much weaker than when a compressive strain in h2 is created. When f2 is zero due to lattice matching to the virtual buffer, the increased stability with increasing h2 comes from the fact that h_i is increasing and therefore decreasing δ (and increasing S).

It will be appreciated that all the calculations are equilibrium calculations, and as usual, one might suspect that these numbers are somewhat conservative, although also consider that the layers possess many threading dislocations that can bend over at the critical thickness, so there are plenty of sources for misfit dislocation generation.

Sacrificial SiGe capping layers provide an innovative method for the protection of thin strained device layers during processing. Such layers shield these critically important strained channel layers from process steps, such as wet chemical cleans and oxidations, which consume surface material. Before the growth or deposition of the gate dielectric, these protective SiGe layers can be selectively removed by standard processes such as oxidation or wet etching, revealing the intact strained device layer. Also presented is a guideline for engineering strained layer stacks such that relaxation via misfit dislocation is prevented. Compressively strained intermediate layers increase the stability of tensile channel layers, and also serve as a barrier for misfit dislocation introduction into the underlying layers.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A semiconductor structure comprising:

a relaxed $Si_{1-x}Ge_x$ layer on a substrate;

a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer; and

a sacrificial $Si_{1-y}Ge_y$ layer.

2. The structure of claim 1, wherein said sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer.

3. The structure of claim 2, wherein said dielectric layer comprises a gate dielectric of a MISFET.

4. The structure of claim 3, wherein the gate dielectric comprises an oxide.

5. The structure of claim 3, wherein the gate dielectric is deposited.

6. The structure of claim 3, wherein the MISFET comprises a surface channel device.

7. The structure of claim 3, wherein the MISFET comprises a buried channel device.

8. The structure of claim 1, wherein the strained channel comprises Si.

9. The structure of claim 1, wherein x is approximately equal to y.

10. The structure of claim 9 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

11. The structure of claim 1, wherein $y > x$.

12. The structure of claim 11 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

13. The structure of claim 12, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

14. The structure of claim 1, wherein the substrate comprises Si.

15. The structure of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

16. The structure of claim 1, wherein the substrate comprises a SiGe graded buffer layer on Si.

17. The structure of claim 1 further comprising a $Si_{1-w}Ge_w$ spacer layer.

18. The structure of claim 17, wherein said sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer.

19. The structure of claim 18, wherein said dielectric layer comprises the gate dielectric of a MISFET.

20. The structure of claim 19, wherein the gate dielectric comprises an oxide.

21. The structure of claim 19, wherein the gate dielectric is deposited.

22. The structure of claim 19, wherein the MISFET comprises a buried channel device.

23. The structure of claim 17, wherein the strained channel comprises Si.

24. The structure of claim 17, wherein w is approximately equal to y.

25. The structure of claim 24 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

26. The structure of claim 17, wherein $y > w$.

27. The structure of claim 26 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

28. The structure of claim 27, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

29. The structure of claim 17, wherein the substrate comprises Si.

30. The structure of claim 17, wherein the substrate comprises Si with a layer of SiO_2.

31. The structure of claim 17, wherein the substrate comprises a SiGe graded buffer layer on Si.

32. The structure of claim 1 further comprising a $Si_{1-w}Ge_w$ spacer layer and a Si layer.

33. The structure of claim 32, wherein said sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer.

34. The structure of claim 33, wherein said dielectric layer comprises the gate dielectric of a MISFET.

35. The structure of claim 34, wherein the gate dielectric comprises an oxide provided by oxidizing said Si layer.

36. The structure of claim 1, wherein y is made greater than x in order to enhance the stability of said semiconductor structure.

37. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer;

removing said $Si_{1-y}Ge_y$ layer; and

providing a dielectric layer.

38. The method of claim 37, wherein said $Si_{1-y}Ge_y$ layer is removed by a selective technique.

39. The method of claim 38, wherein said selective technique is wet oxidation below 750°C.

40. The method of claim 38, wherein said selective technique is a wet or dry chemical etch.

41. The method of claim 37, wherein said dielectric layer comprises a gate dielectric of a MISFET.

42. The method of claim 41, wherein the gate dielectric comprises an oxide.

43. The method of claim 41, wherein the gate dielectric is deposited.

44. The method of claim 41, wherein the MISFET comprises a surface channel device.

45. The method of claim 41, wherein the MISFET comprises a buried channel device.

46. The method of claim 37, wherein the strained channel layer comprises Si.

47. The method of claim 37, wherein x is approximately equal to y.

48. The method of claim 47 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

49. The method of claim 37, wherein $y > x$.

50. The method of claim 49 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

51. The method of claim 50, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

52. The method of claim 37, wherein the substrate comprises Si.

53. The method of claim 37, wherein the substrate comprises Si with a layer of SiO_2.

54. The method of claim 37, wherein the substrate comprises a SiGe graded buffer layer on Si.

55. The method of claim 37, wherein the semiconductor device comprises a MISFET.

56. The method of claim 37, wherein said $Si_{1-y}Ge_y$ layer is removed to expose said strained channel layer.

57. The method of claim 37, wherein said heterostructure further comprises a $Si_{1-w}Ge_w$ spacer layer.

58. The method of claim 57, wherein said dielectric layer comprises the gate dielectric of a MISFET.

59. The method of claim 58, wherein the gate dielectric comprises an oxide.

60. The method of claim 58, wherein the gate dielectric is deposited.

61. The method of claim 58, wherein the MISFET comprises a buried channel device.

62. The method of claim 57, wherein the strained channel comprises Si.

63. The method of claim 57, wherein y is approximately equal to w.

64. The method of claim 63 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

65. The method of claim 57, wherein $w > y$.

66. The method of claim 65 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

67. The method of claim 66, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

68. The method of claim 57, wherein the substrate comprises Si.

69. The method of claim 57, wherein the substrate comprises Si with a layer of SiO_2.

70. The method of claim 57, wherein the substrate comprises a SiGe graded buffer layer on Si.

71. The method of claim 57, wherein the semiconductor device comprises a MISFET.

72. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$

layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

providing a dielectric layer.

73. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

oxidizing said Si layer.

74. The method of claim 73, wherein the semiconductor device comprises a MOSFET.

75. The method of claim 73, wherein the semiconductor device comprises a buried channel MOSFET.

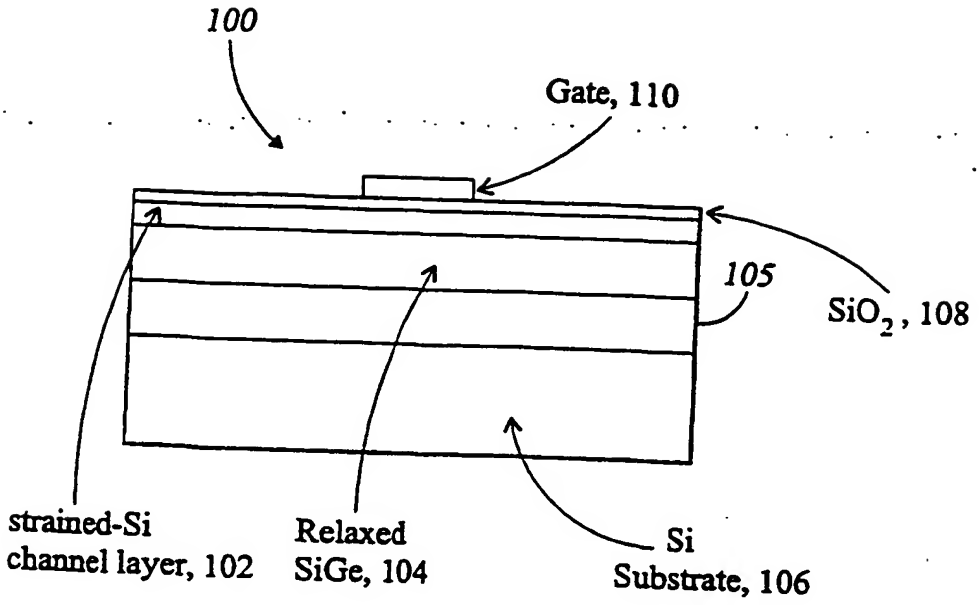
100
Gate, 110
105
SiO_2, 108
strained-Si
channel layer, 102
Relaxed
SiGe, 104
Si
Substrate, 106

FIG. 1A

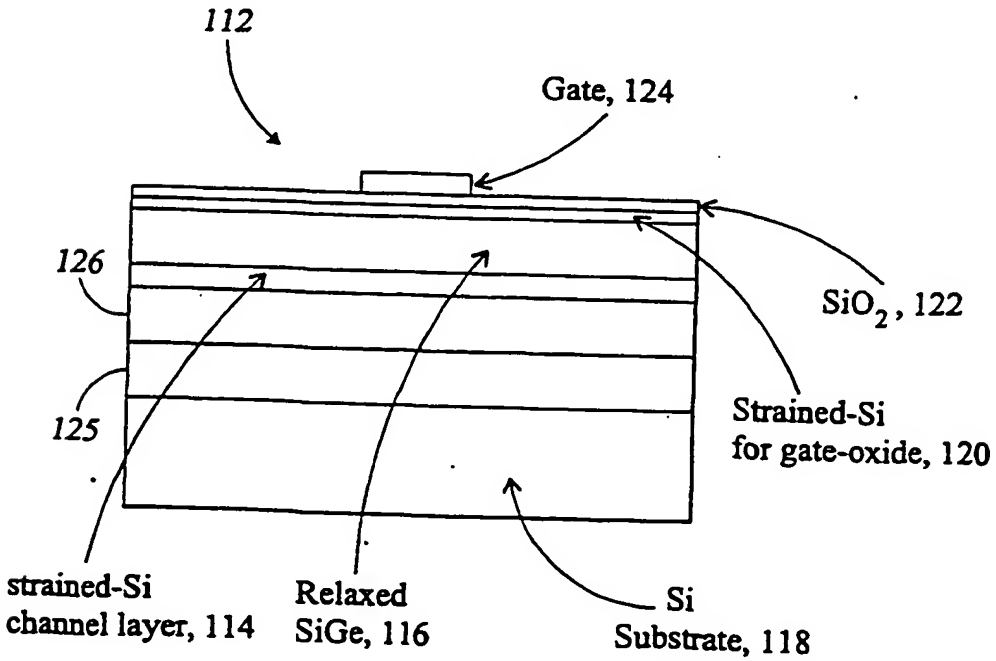
112
Gate, 124
126
SiO_2, 122
125
Strained-Si
for gate-oxide, 120
strained-Si
channel layer, 114
Relaxed
SiGe, 116
Si
Substrate, 118

FIG. 1B

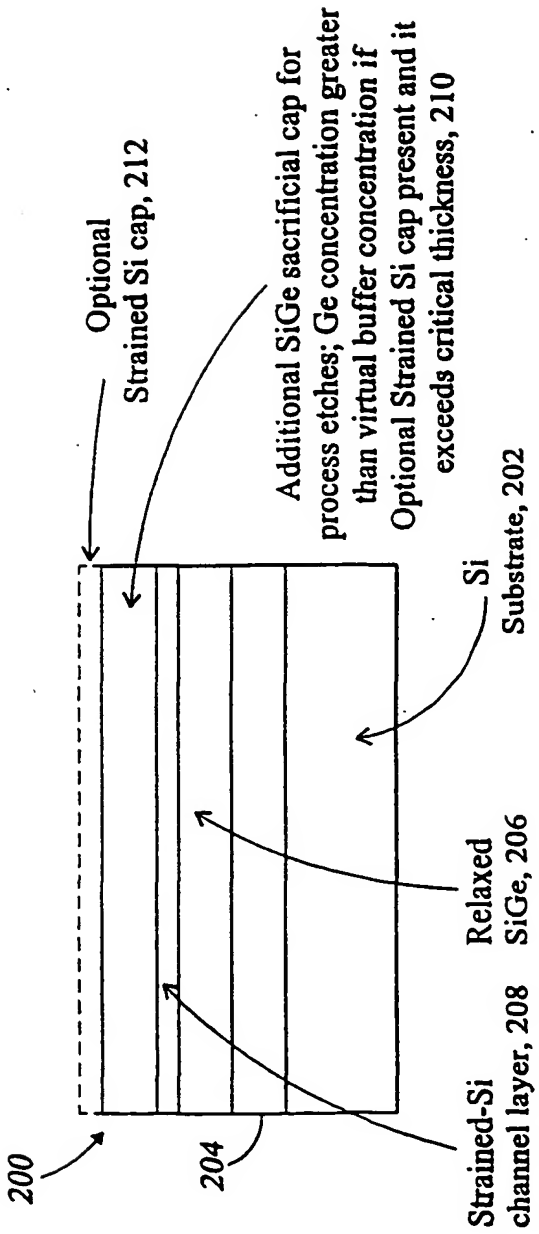
Optional
Strained Si cap, 212
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 210
Si
Substrate, 202
Relaxed
SiGe, 206
Strained-Si
channel layer, 208
204
200

FIG. 2A

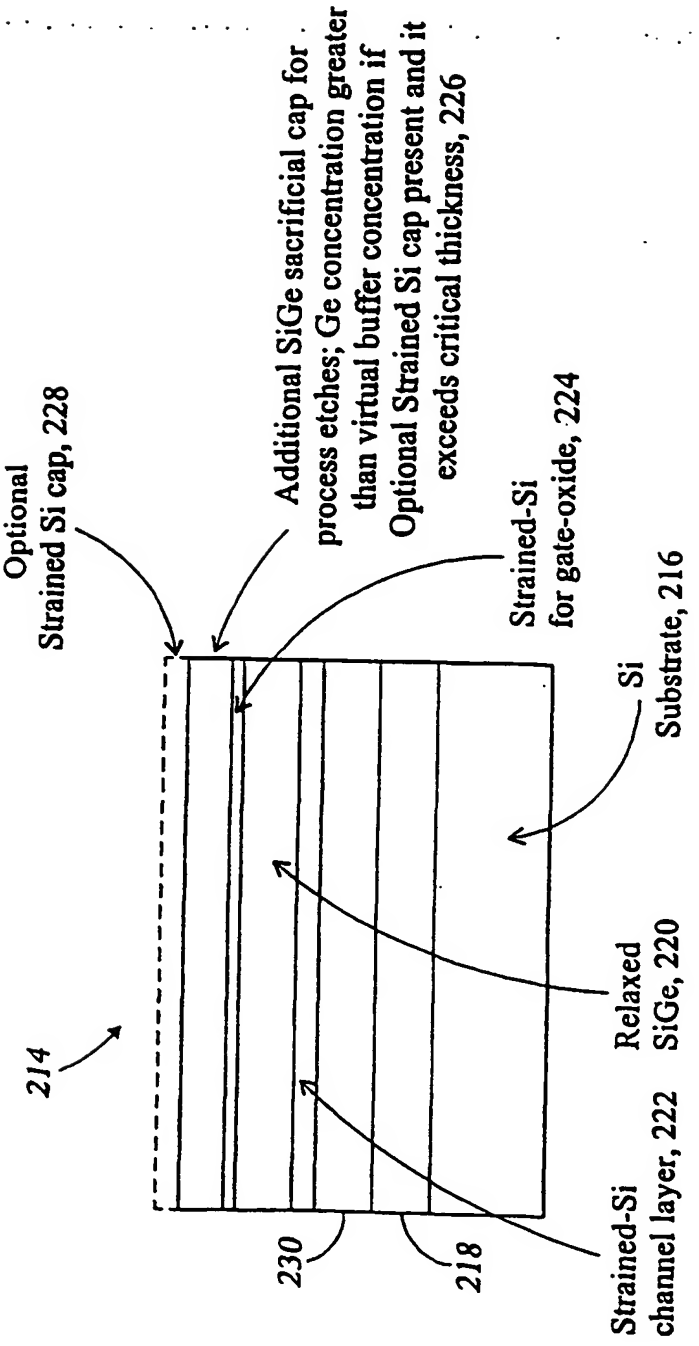
Optional
Strained Si cap, 228
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 226
Strained-Si
for gate-oxide, 224
Si
Substrate, 216
Relaxed
SiGe, 220
214
230
218
Strained-Si
channel layer, 222

FIG. 2B

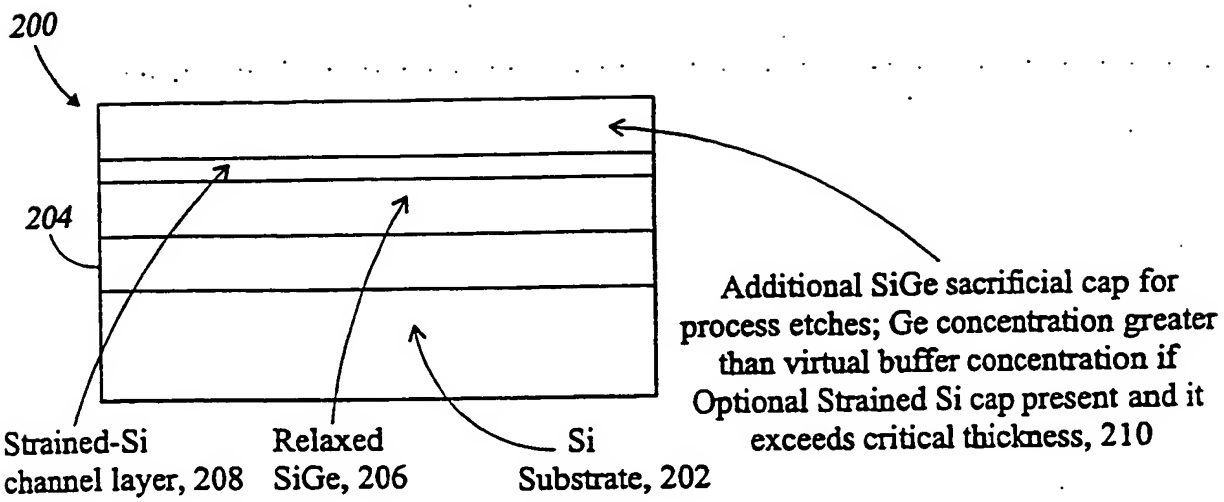
200
204
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 210
Strained-Si channel layer, 208
Relaxed SiGe, 206
Si Substrate, 202

FIG. 3A

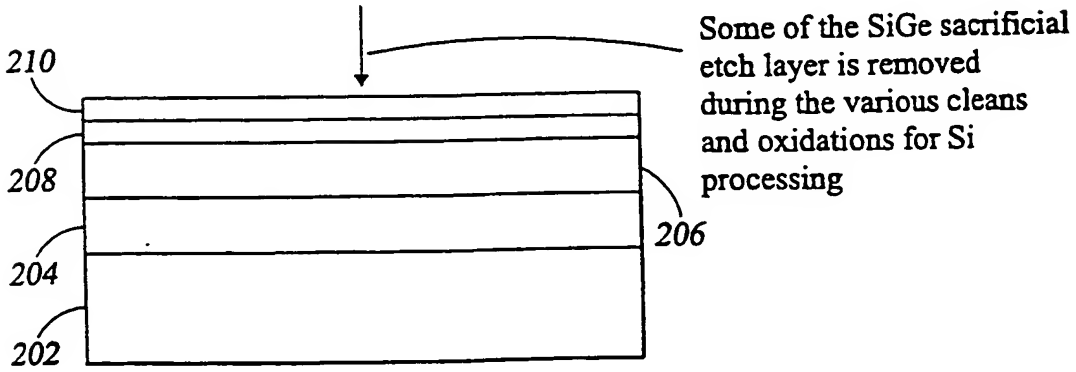
Some of the SiGe sacrificial etch layer is removed during the various cleans and oxidations for Si processing
210
208
206
204
202

FIG. 3B

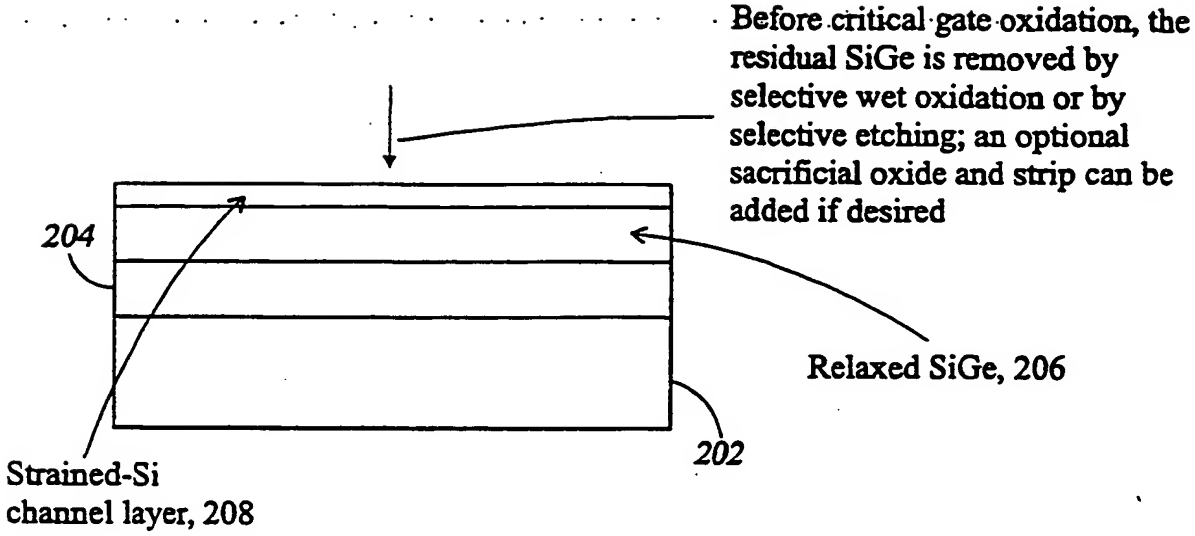
Before critical gate oxidation, the residual SiGe is removed by selective wet oxidation or by selective etching; an optional sacrificial oxide and strip can be added if desired
204
Relaxed SiGe, 206
202
Strained-Si channel layer, 208

FIG. 3C

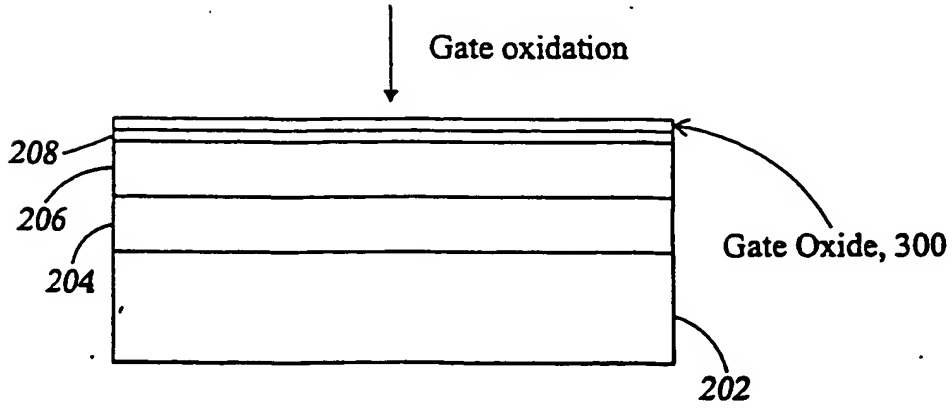
Gate oxidation
208
206
204
Gate Oxide, 300
202

FIG. 3D

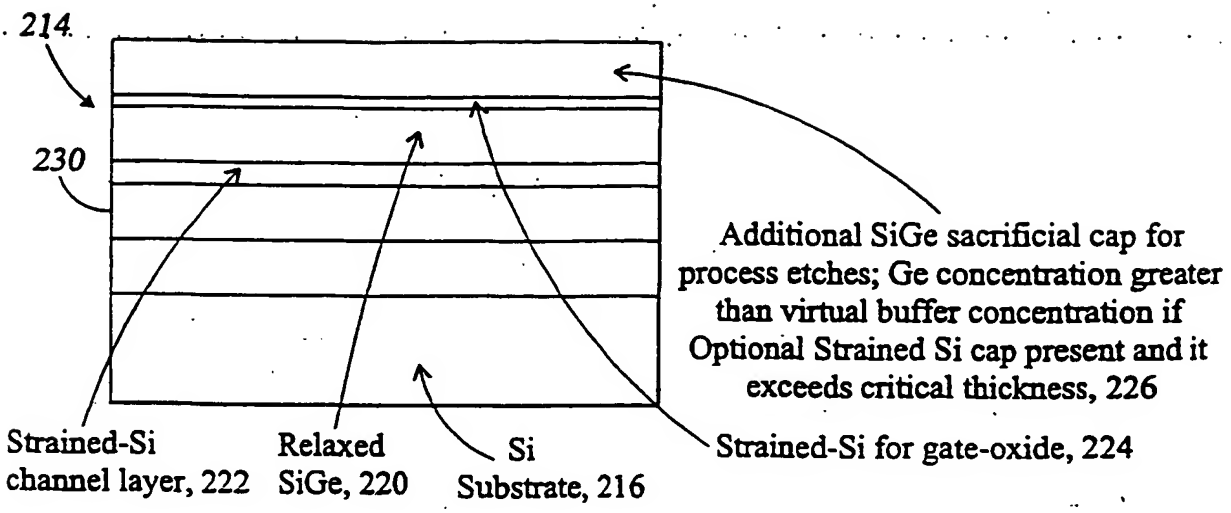
214
230
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 226
Strained-Si channel layer, 222
Relaxed SiGe, 220
Si Substrate, 216
Strained-Si for gate-oxide, 224

FIG. 4A

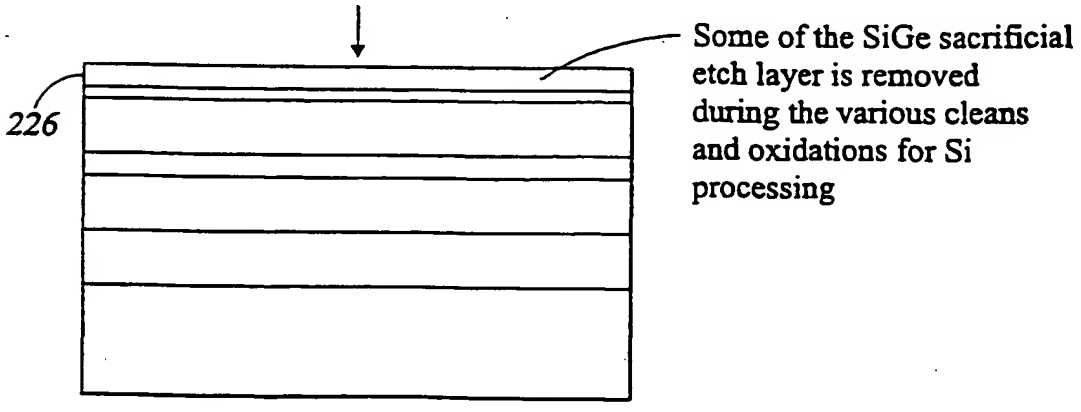
226
Some of the SiGe sacrificial etch layer is removed during the various cleans and oxidations for Si processing

FIG. 4B

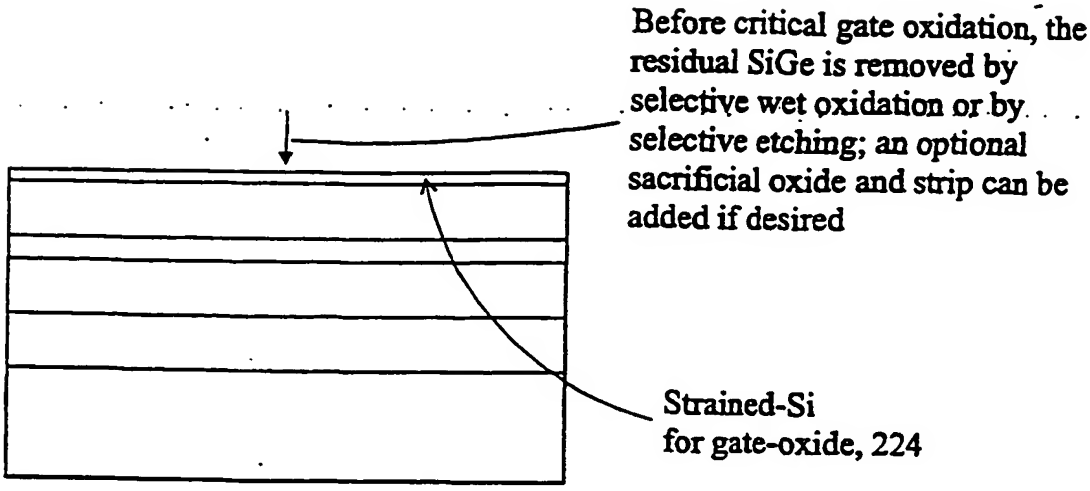
Before critical gate oxidation, the residual SiGe is removed by selective wet oxidation or by selective etching; an optional sacrificial oxide and strip can be added if desired
Strained-Si for gate-oxide, 224

FIG. 4C

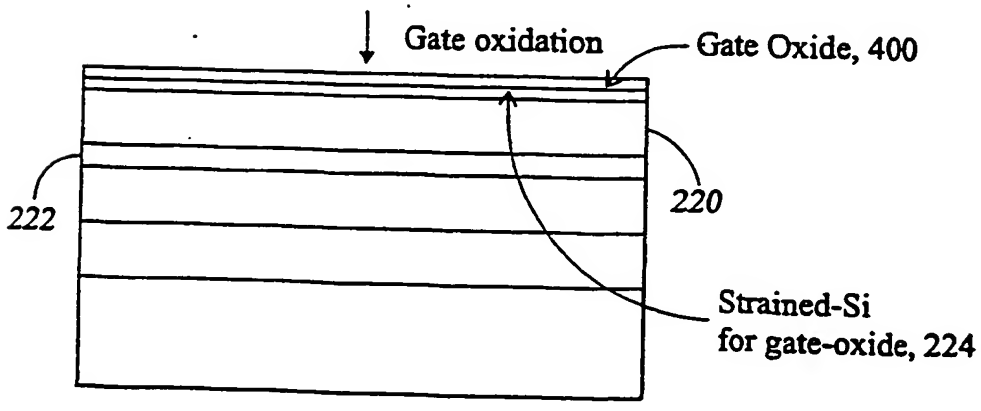
Gate oxidation
Gate Oxide, 400
222
220
Strained-Si for gate-oxide, 224

FIG. 4D

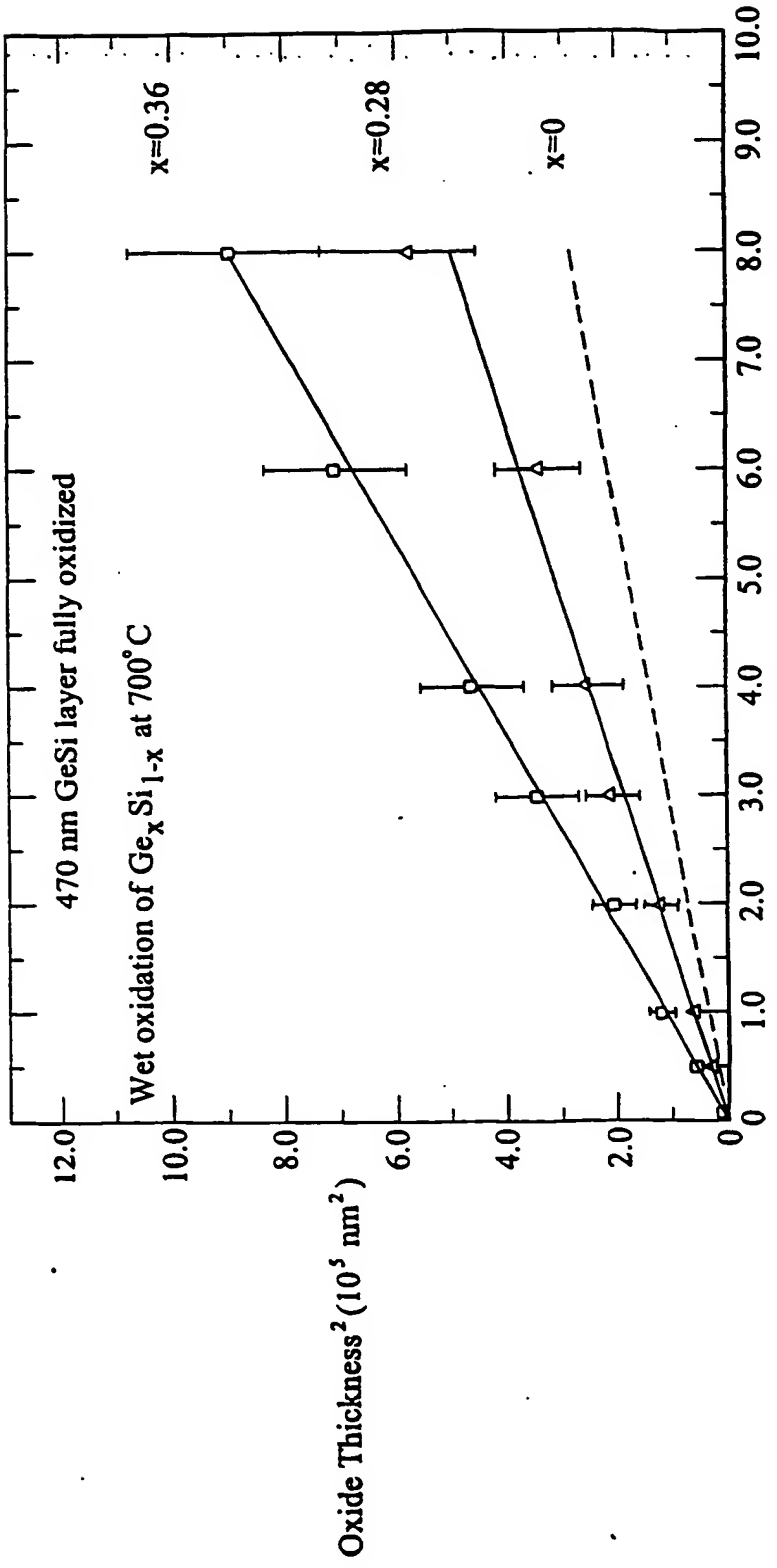
Wet oxidation of Ge_xSi_{1-x} at 700°C
470 nm GeSi layer fully oxidized
x=0.36
x=0.28
x=0
Oxide Thickness^2 (10^5 nm^2)
Oxidation Duration (hr)
0
2.0
4.0
6.0
8.0
10.0
12.0
1.0
3.0
5.0
7.0
9.0

FIG. 5

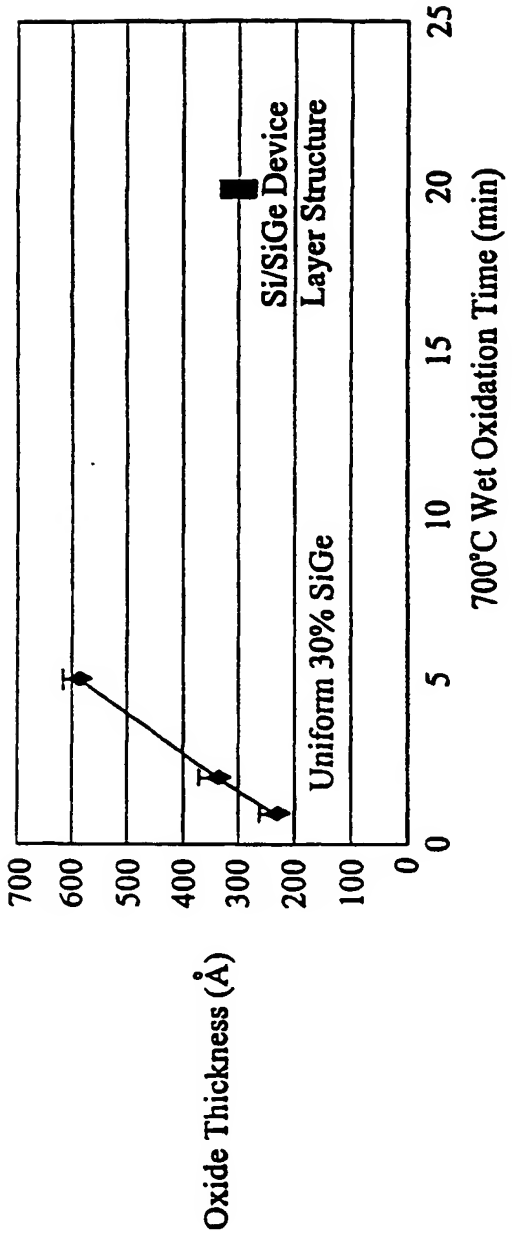
Oxide Thickness (Å)
700
600
500
400
300
200
100
0
0
5
10
15
20
25
700°C Wet Oxidation Time (min)
Uniform 30% SiGe
Si/SiGe Device
Layer Structure

FIG. 6

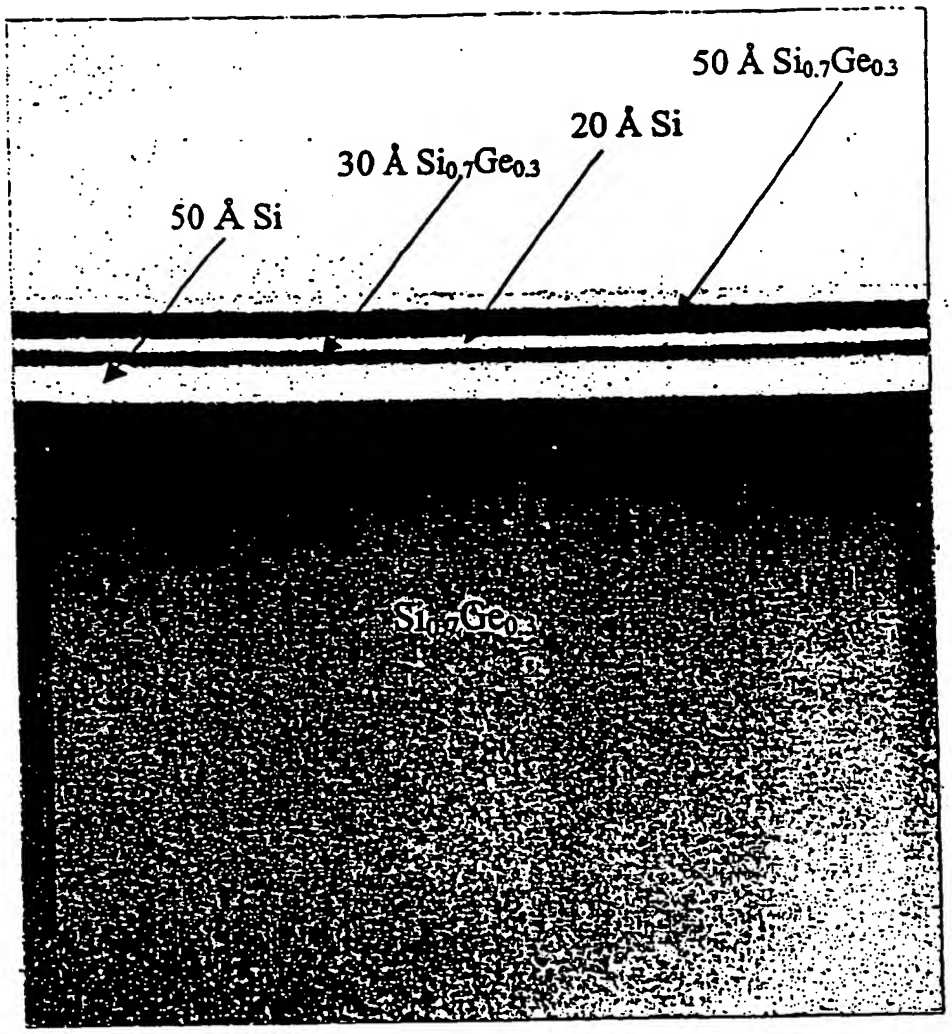

FIG. 7

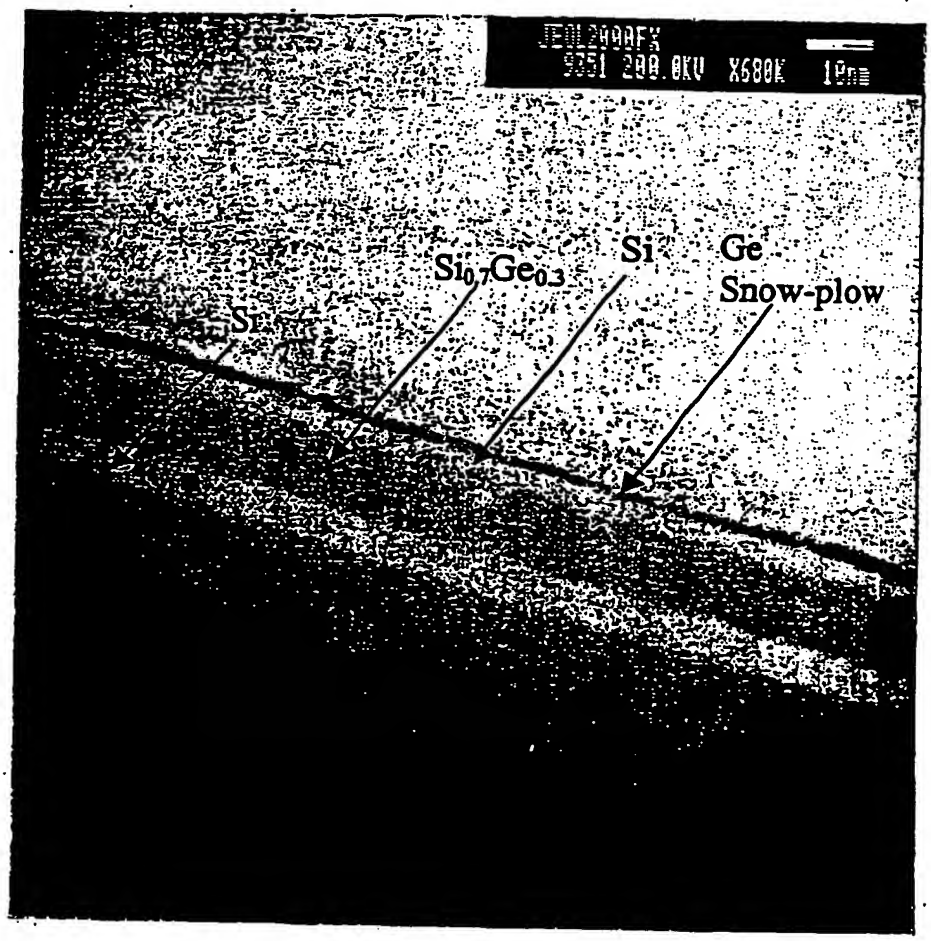
JEOL2000FX
9251 200.0KV X680K 10nm
Si
$Si_{0.7}Ge_{0.3}$
Si
Ge
Snow-plow

FIG. 8

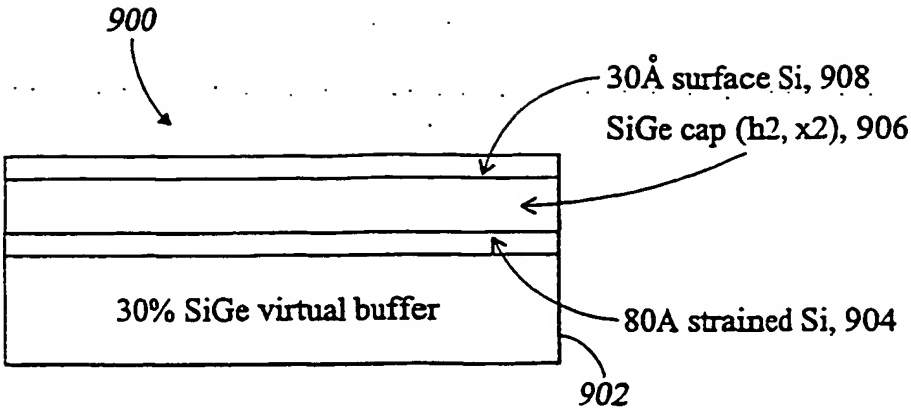
900
30Å surface Si, 908
SiGe cap (h2, x2), 906
30% SiGe virtual buffer
80A strained Si, 904
902

FIG. 9

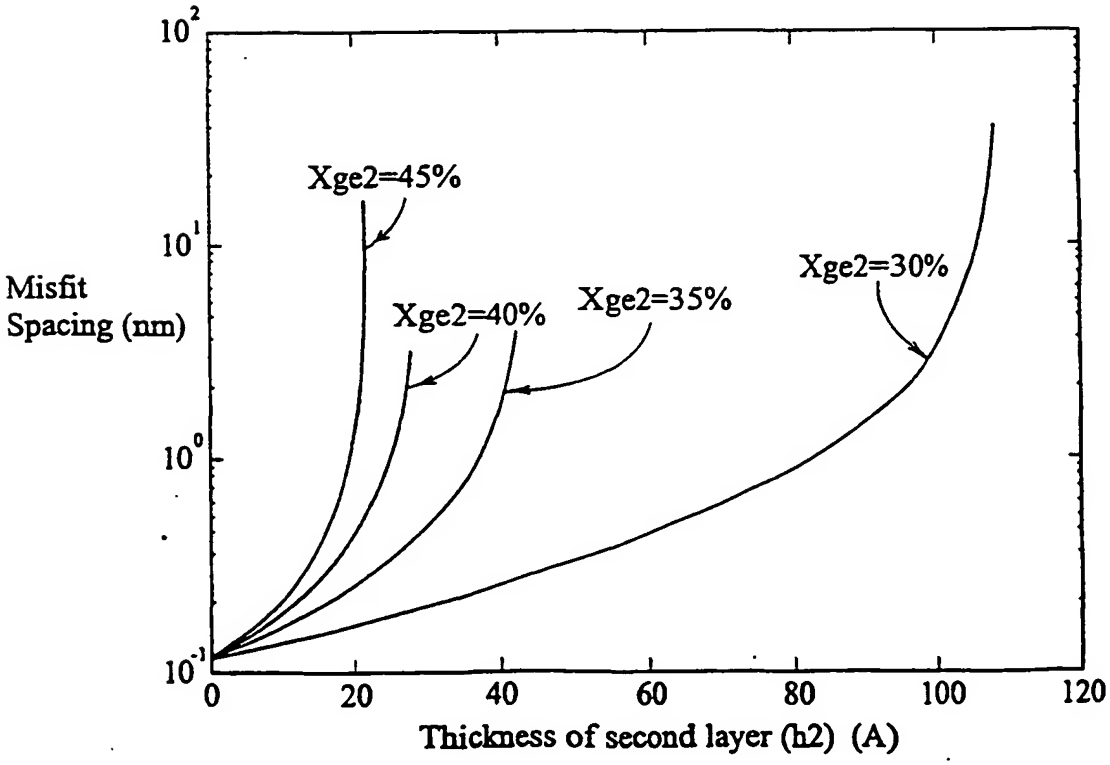
Misfit
Spacing (nm)
Xge2=45%
Xge2=40%
Xge2=35%
Xge2=30%
Thickness of second layer (h2) (A)

FIG. 10

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(74) Agent: CONNORS, Matthew, E.; Samuels, Gauthier & Stevens, LLP, 225 Franklin Street, Suite 3300, Boston, MA 02110 (US).

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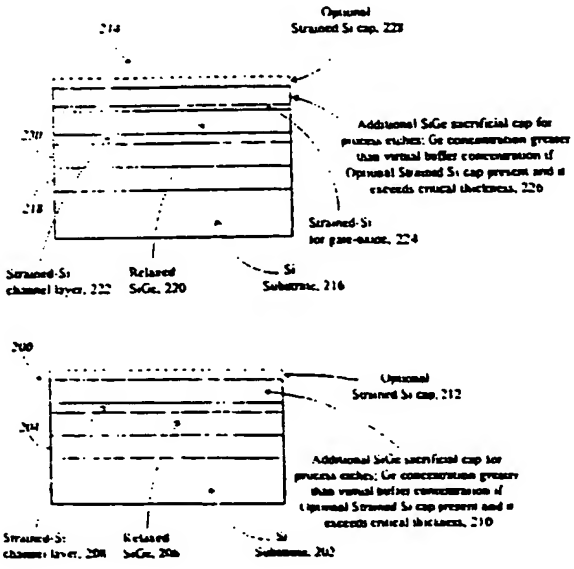
Published:
— *with international search report*

[Continued on next page]

(54) Title: GATE TECHNOLOGY FOR STRAINED SURFACE CHANNEL AND STRAINED BURIED CHANNEL MOSFET DEVICES



(57) Abstract: A semiconductor structure including a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a sacrificial $Si_{1-y}Ge_y$ layer. The sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer. The dielectric layer includes a gate dielectric of a MOSFET. In alternative embodiements, the structure includes a $Si_{1-z}Ge_z$ spacer layer and a Si layer. In another embodiment of the invention there is provided a method of fabricating a semiconductor device including providing a semiconductor heterostructure, the heterostructure having a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on the relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer; removing the $Si_{1-y}Ge_y$ layer; and providing a dielectric layer.

WO 02/13262 A3

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) **Date of publication of the international search report:**
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INTERNATIONAL SEARCH REPORT

Intern* ...al Application No
PCT/US 01/24614

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/10 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 683 522 A (IBM) 22 November 1995 (1995-11-22) figures 2,3	1-75
X	EP 0 587 520 A (IBM) 16 March 1994 (1994-03-16) figure 2	1-75
X	JP 2000 031491 A (HITACHI LTD) 28 January 2000 (2000-01-28) figures 8,10-12	1-75

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Date of the actual completion of the international search	Date of mailing of the international search report
1 March 2002	11/03/2002

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